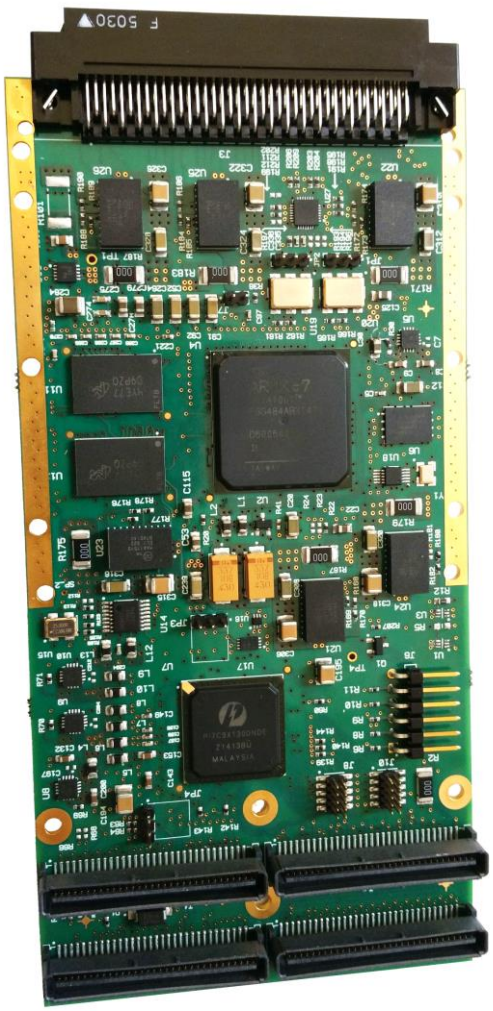
Data sheet

DPIO2



Hardware characteristics

The LVD_DPIO2 is an FPGA based PMC module that implements a general purpose LVDS receiver/transmitter. It features:

- up 133 MHz PCI-X 64 bit bus
- Artix7 XC7A100T
- 128 Mbit of bitstream configuration QSPI memory
- Programmable clock generator : from 2.5 kHz e 200 MHz (SI5351A-B)
- 1 GB DDR3L memory
- 80 ways front panel connector
- Additional 64 IOs on PMC J14 (32 differential)

Performance:

- Maximum PCI bandwidth : 1GB/s theorical
- Maximum DDR memory bandwidth : 5GB/s theorical

Please contact directly LVD Systems for any other information needed for this product

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